IN THE SPECIFICATION

In the Drawings

The drawings are objected to as failing to include reference characters and darkened or black regions. Applicant has amended the drawings accordingly and submitted formal drawings. No new matter has been added.

In the Specification

Please replace paragraph [0014] with the following:

[0014] Figures 1-2 compare actual sizes of exemplary RFID filaments or threads made in accordance [[to]] with embodiments of the present invention to a U.S. dime;

Please replace paragraph [0021] with the following:

[0021] Figure 10 illustrates exemplary dimensions of an RFID tag made in accordance [[to]] with embodiments of the present invention;

Please replace paragraph [0023] with the following:

[0023] Figure 12 illustrates an exemplary embodiment of assembling RFID tags in accordance [[to]] with some ~~embodiment~~ embodiments of the present invention;

Please replace paragraph [0024] with the following:

[0024] Figures 13A-13B illustrate another exemplary embodiment of assembling RFID tags in accordance [[to]] with some ~~embodiment~~ embodiments of the present invention;

Please replace paragraph [0032] with the following:

[0032] In one embodiment we describe a form factor for RFID tags, in which the RFID tag is in the form of a thin, flexible strip, reminiscent of a filament 10 or a thread 20. Throughout the document, the RFID devices in the form of such thin, flexible strip, filament, thread, or other suitable structures are referred to as "RFID tags." These RFID tags can be quite small (**Figures 1 and 2**). **Figures 1 and 2** show photographic examples of electronic assemblies for RFID applications comparing the filament 10 and thread 20 of RFID to a U.S. dime 11. **Figures 3 and 4** illustrate that in one embodiment, an RFID tag 20 comprises a flexible substrate 28 (in one embodiment, a plastic film), an integrated circuit 26 embedded within the flexible substrate 28, and two conductive films 22 and 24 formed on top of the flexible or plastic substrate 28. The conductive films 22 and 24 are in electrical connection to the integrated circuit 26 that serve as antennas.

Please replace paragraph [0034] with the following:

[0034] **Figures 5A-5C** illustrate more examples of an RFID tag having a filament structure 10 using a NanoBlock™ IC as an integrated circuit 26. NanoBlock™ is a trademark of Alien Technology Inc. For clarity ~~purpose~~ purposes, the printed conductors are not shown. **Figures 5B-5C** show the top and bottom view of the RFID tag with the integrated circuit 26.

Please replace paragraph [0037] with the following:

[0037] In one embodiment, a singulation process is used to separate the array of tags into individual RFID tags; in one exemplary embodiment, the singulation process may be performed by mechanical cutting, sawing, punching, laser ablating, hot-blade knife cutting or other techniques. After the singulation process is completed, an individual RFID tag may look like the RFID tag 20 shown in **Figure 3**. Exemplary dimensions of these tags produced from the plastic sheet 60 are described below and shown also in **Figure 10**. It can be seen from **Figure 6** that there are subarrays of RFID tags which are separated from each other by saw-tooth shaped gaps 63. It can also be seen that the ICs 62 are deposited in lines which are parallel to the edges of the plastic sheet 60 which may be, in one

exemplary embodiment, processed as a web material in a roll to roll web process, such as a type of process which is used to make paper. In one embodiment, the printed conductive traces 64, which are used to form the antenna elements for each tag, are formed at an oblique angle relative to the edges of the plastic sheet 60. In the case of **Figure 6**, each conductive trace forms an angle of about 10°. This arrangement tends to optimize (e.g. maximize) the amount of filament RFID tags which can be fabricated in a given area of the plastic sheet 60. It will be appreciated that different layouts, [[(]]such as angle of the trace relative to the edge of the web material (which will engage the rolls at the beginning and end of the process) may be optimal for RFID tags of different lengths and widths. As shown in **Figure 6**, the ends of one group of subarrays, such as the group of subarrays 65, interdigitate or interlace with the ends of an adjacent group of subarrays 66; this additional layout arrangement also tends to maximize the amount of filament RFID tags (or other types of devices) which can be fabricated in a given area of the plastic sheet. The ends of each conductive trace are adjacent to the gaps 63.

Please replace paragraph [0044] with the following:

[0044] In one embodiment, the RFID tag is deployed (or incorporated) or configured to deploy into another item in a way that the RFID tag spans into a three dimensional structure, e.g., an RFID thread bent into a curved RFID filament or thread or an RFID thread shaped or bent into a wrinkled RFID thread or otherwise an RFID tag shaped in a three dimensional structure. There are a variety of ways of constructing an RFID tag to include [[of]] integrated circuits, flexible polymers, flexible substrate, and conductive traces. Following are some illustrative examples. While these structures can be used for narrow filament tags, it should also be recognized that more conventional RFID tag structures can also be built using these structures.

Please replace paragraph [0045] with the following:

[0045] **Figure 7** shows, in a cross-sectional view, one construction of an RFID tag. An RFID tag shown in **Figure 7** can be one of the RFID tag shown in **Figure 6**. In one exemplary method for forming this structure, an integrated circuit 71 is deposited in a receptor hole 73 in the base film (a

flexible or plastic substrate 75) using an FSA process. In one embodiment, the integrated circuit 71 is positioned or deposited such that it is coplanar with the flexible substrate 75. In one embodiment, coplanar refers to a configuration where the integrated circuit 71 is deposited in the substrate 75 such that a surface of the integrated circuit 71 is flushed flush with a surface of the substrate 75. In one embodiment, coplanar refers to a configuration where the integrated circuit 71 is deposited in the substrate 75 such that a surface of the integrated circuit 71 is below a surface of the substrate 75. In one embodiment, coplanar refers to a configuration where the integrated circuit 71 is deposited in the substrate 75 such that a top surface of the integrated circuit 71 shares essentially the same plane as the top surface of the substrate 75.

Please replace paragraph [0046] with the following:

[0046] Still with **Figure 7**, a planarization layer 77, which may comprise a polymer, is formed on top of the substrate 75 and integrated circuit 71. Via holes 72 are formed in the planarization layer to expose the contact pads (not shown) on the integrated circuit 71. A metal interconnection 79 (or metal traces, or conductive elements, or antenna elements) is then made to both provide a connection to the pads on the integrated circuit as well as to form antennas for the RFID tag. While photolithographic methods can be used to form the metal traces it is also possible to simply print conductive inks on the substrate 75 to form the antennas. This printing operation simultaneously forms an electrical connection to the integrated circuit 71 and forms the antenna elements. The metal interconnection 79, the conductive elements, the conductive traces, or the antenna can be formed by screen printing, ink jet printing, or extrusion printing. The RFID tag shown in **Figure 7** may be similar to the tag 20 shown in **Figure 3**. It is to be noted that the RFID tag shown in **Figure 7** is not drawn to scale. The metal interconnection 79, the conductive elements, the conductive traces, or the antenna can be any one of a printed conductive element, evaporated metal, sputtered metal, plated metal, or laminated conducting foil.

Please replace paragraph [0052] with the following:

[0052] Figure 10 shows some illustrative dimensions for a filament RFID tag where the substrate which holds an IC 101 of the RFID tag is not shown. In one embodiment, the substrate may be only minimally wider than the antenna elements 104 and 105. The

antenna elements 104 and 105 are shown electrically coupled to the IC 101 through bonding pads 106 and [[107]] 199.

Please replace paragraph [0056] with the following:

[0056] Figure 11 illustrates an exemplary embodiment where an RFID IC can be assembled into a substrate where proper alignment or orientation of the RFID IC to be deposited into a receptor in the substrate is more relaxed or less stringent. As shown in **Figure 11**, an RFID IC 110 is placed into a receptor 109 which includes a conductive element 117 that serves as an antenna element. The conductive element 117 is thus located [[is]] below the RFID IC 110. This conductive element 117 may be referred to as a bottom antenna and it is electrically coupled (resistively or capacitively) to the IC 110. The RFID IC 110 is also electrically coupled (resistively or capacitively) to a conductive element 107 which is above the RFID IC, and the conductive element 107 may be referred to as a top antenna. In one embodiment, the RFID IC 110 is electrically coupled to the top antenna through a contact 116 provided on a top surface of the RFID IC 110 and is electrically coupled to the bottom antenna through a contact 115 provided on a bottom surface of the RFID IC 110.

Please replace paragraph [0058] with the following:

[0058] In one embodiment of this RFID tag, the size of the top contact 116 on a top surface of the RFID IC is significantly larger than a bonding pad 136 on the top of the RFID IC 110, and the size of the bottom contact 115 on the bottom surface of the RFID is significantly larger than another bonding pad 137 on the top of the RFID IC 110. In this embodiment, the size of the top contact 116 is about the same size as the entire top surface of the RFID IC 110, and the size of the bottom contact 115 is about the same size as the entire bottom surface of the RFID IC 110. In one embodiment, the RFID IC 110 includes an interconnect 115a which extends from a bonding pad 137 on the top of the IC 110, around a side of the IC 110 to the bottom of the IC 110, and the bottom portion of this interconnect 115a may be the bottom contact 115. In one embodiment, the RFID tag may include a planarization layer or a ~~dialectic~~ dielectric layer (not shown) formed on top of the spacer layer 120 and the IC 110 similar to the RFID tag shown in **Figure 7**.

Please replace paragraph [0059] with the following:

[0059] The RFID IC 110 is supported, in one embodiment, within a spacer layer 120 which is coupled to the top antenna 107 and to the bottom ~~antenna117~~ antenna 117. The receptor or opening 109 in the spacer layer 120 is considerably larger than the size of the RFID IC 110. This opening 109 is not designed to relatively precisely match the size of the block of the RFID IC 110. Rather, the RFID IC 110 fits in the opening 109 without aligning to the perimeter of the opening 109. In one exemplary embodiment the opening is at least 50% larger in area than the area of the bottom surface (or area of the top surface) of the block of the RFID IC 110. Further, the geometry of the opening 109 does not need to match the geometry of the RFID IC 110; for example, the opening 109 may have a circular geometry and the RFID IC 110 may have a rectangular (e.g., square) geometry. Even though an FSA process may be used to place the RFID ICs 110 into the openings 109, the RFID ICs 110 do not need to be aligned to the perimeter of the opening 109. Thus, after an FSA process, the RFID ICs 110 may have different rotational orientations within the openings 109. The RFID ICs 110 in this embodiment are designed to operate properly whether they are oriented up or down (relative to the layer of circuitry in the RFID IC 110) because there is only one electrical contact on a top surface of the RFID IC 110 (contact 116) and only one electrical contact on a bottom surface of the RFID IC 110 (contact 115). Since these contacts cover a large portion of both surfaces (top and bottom) of the RFID IC 110 and since there are no other electrical contacts on these surfaces, it is possible to deposit the RFID ICs 110 into the openings 109 without aligning them in the openings 109 and without needing to align small bonding pads on the RFID ICs 110 to interconnects on the top and bottom antennas. The embodiments discussed may be used for thread tags or non-thread tags. These embodiments ~~allows~~ allow an FSA process in which blocks, each containing a functional element (e.g. an RFID IC), are mixed in a fluid to form a slurry and then the slurry is deposited onto a substrate having openings wherein the openings are substantially larger and/or having different shapes than the blocks and/or the perimeters of the blocks are not aligned with the perimeters of the openings after the FSA process is completed.

Please replace paragraph [0062] with the following:

[0062] Next, the RFID NanoBlock™ device 110 is deposited in a substrate to form an RFID tag. In one embodiment, the RFID tag is formed on a web-base material or substrate and then singulated into an individual RFID tag. Thus, a plurality of RFID tags can be formed on one substrate. **Figure 12** illustrates an exemplary embodiment of assembling RFID tags in accordance [[to]] with some ~~embodiment~~ embodiments of the present invention. In one embodiment, an FSA process is used to assemble a plurality of RFID ICs into the substrate of the RFID tags. The spacer layer 120 is adhered to a substrate that is a web-based material. In **Figure 12**, a substrate 129 having one or more strips of a NanoBlock™ spacer layer 120 in which NanoBlock™ device receptor site holes 121 have been formed is provided. The substrate 129 may have a form of a web substrate as shown in **Figure 12**. The cut-off end of the web substrate is to indicate that what is shown in the figure is a section from a long web (processed in a roll to roll web process, such as a paper making process).

Please replace paragraph [0063] with the following:

[0063] As shown in **Figure 12,** the holes 121 have a circular shape. These circular holes 121 can be fabricated by punching, embossing, drilling, laser cutting or ablation, etc. The holes 121 may have alternative geometries such as rectangular or square holes or have other regular shapes or even be irregularly shaped. To facilitate assembly, the spacer layer 120 may be coated on its front and/or back side with an adhesive material, such as a PSA, hot-melt adhesive, etc, or non-conducting b-staged epoxy or a UV-curable polymeric material (not shown). The thickness of this spacer layer 120 and the size of the holes 121 are made such that no more [[that]] than one NanoBlock™ device 110 will remain in each hole 121 after completion of the FSA process.

Please replace paragraph [0068] with the following:

[0068] Depending on the location and type of adhesive materials employed, the NanoBlock™ devices 110, if desired, might now be attached to the substrate assembly by

a hot-roll lamination process. In one embodiment, the spacer layer [[132]] 120 is semi-transparent. The substrate assembly includes (as shown in **Figure 14A**) three strips of spacer layers 120 laminated onto a bottom antenna layer 130. It is to be expected that more or less than three spacer layers [[132]] 120 maybe included. In one embodiment, each strip of spacer layer 120 is aligned over one of the conducting adhesive strips 132 which are adhered onto the [[bottom-antenna-layer]] bottom antenna layer 130.

Please replace paragraph [0069] with the following:

[0069] **Figure 14B** shows a close-up cross-section of a NanoBlock™ device 110 in a receptor site (hole 121) formed by an assembly of a strip of spacer layer (e.g. spacer layer 120) and the [[bottom-antenna-layer]] bottom antenna layer (e.g. layer 130). In one embodiment, individual spacer layer strips 120 are laminated over individual conducting adhesive strip 132 which is adhered on the [[bottom-antenna-layer]] bottom antenna layer 130. Alternatively, the spacer layer strips 120 are laminated over one continuous adhesive strip 132. As noted in **Figure 12**, the adhesive layers 132 on the top and bottom of the spacer layer strip 120 are employed to hold the assembly together, and the NanoBlock™ device 110 is held in place by a portion of the conducting adhesive strip 132 originally part of the bottom-antenna-layer 130.

Please replace paragraph [0070] with the following:

[0070] Next, as shown in **Figure 15**, in one embodiment, a top-antenna layer 135 is laminated over the spacer layer 120 that has the RFID IC 110 deposited therein. In one embodiment, the [[top-antenna-layer]] top antenna layer 135 is fabricated of a conducting material or is a layered structure that includes a conducting layer 136 and has a structure, in one embodiment, which is similar to or the same as the structure of the bottom antenna layer 130. In one exemplary embodiment, the top antenna layer 135 includes a conducting layer 136, which may be supported on a plastic substrate (not shown) and conductive adhesive strips 132 adhered to the conducting layer 136. The conductive adhesive strips 132 on the top antenna layer may be arranged in the same pattern as in the case of the bottom antenna layer (see, e.g. **Figure 14A**). With the presence of an adhesive layer that is

conductive as the conductive adhesive strips 132, the conducting layer 136 may be eliminated.

Please replace paragraph [0075] with the following:

[0075] The RFID tag includes a wide spacer layer 180, an additional strip of conducting adhesive 183, applied to either the [[top]] bottom antenna layer 181 or ~~bottom~~ top antenna-layer 182. The RFID tag assembly shown in **Figure 19** is similar to the tag assembly shown in **Figure 15** and includes the bottom antenna layer 181 (which has a conducting layer which serves as the bottom antenna and a conducting adhesive strip which electrically connects the bottom antenna to the bottom contact on the RFID IC 110) and the top antenna layer 182 (which has a conducting layer which serves as the top antenna and a conducting adhesive strip which electrically connects the top antenna to the top contact on the IC 110) and a wide spacer layer 180 which includes an opening to receive the RFID IC 110.

Please replace paragraph [0076] with the following:

[0076] During the top-antenna-layer 182 lamination, the [[top]] bottom antenna layer 181 and the ~~bottom~~ top antenna layers 182 are electrically joined along the added conducting adhesive 183 strip. In the finished tag, the conduction path around the wide spacer layer 180 forms an inductor loop in parallel with the RFID IC 110 (e.g., a NanoBlock™ device), thus enhancing electrical performance in certain embodiments.